UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,372	04/09/2004	Anders Landin	5181-94901	1210

58467 7590 07/09/2008

MHKKG/SUN
P.O. BOX 398
AUSTIN, TX 78767

EXAMINER	
ELAND, SHAWN	

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
07/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/821,372
Filing Date: April 09, 2004
Appellant(s): LANDIN ET AL.

Stephen Curran
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/27/08 appealing from the Office action mailed 12/26/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,434,993	Liencres	7-1995
6,970,872	Chandrasekaran	11-2005
6,065,092	Roy	5-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Liencres*** (5,434,993) in view of ***Chandrasekaran*** (US 6,970,872) and ***Roy*** (US 6,065,092).

In regards to claim 1, Liencres teaches a node including an active device ***(see element 21)***, a system memory ***(see element 37)***, and an interface interconnected by an address network and a data network ***(see element 31)***; an additional node coupled to send a coherency message to

the interface in the node via an inter-node network, wherein the coherency message requests an access right to a coherency unit ***(see figure 3a; see column 6, lines 11 – 15)***.

In regards to claim 13, Liencres teaches a plurality of devices including a system memory ***(see element 37)***, an active device ***(see element 21)***, and an interface configured to send and receive coherency messages on an inter-node network coupling nodes in the multi-node system ***(see element 31)***; an address network configured to convey address packets between the plurality of devices ***(see element 33)***; a data network configured to convey data packets between the plurality of devices ***(see element 33)***.

In regards to claim 24, Liencres teaches an interface in the node receiving a coherency message requesting an access right to a coherency unit via the inter-node network from an additional interface in the additional node ***(see element 33)***.

For claims 1, 13, & 24, Liencres does not teach wherein in response to the coherency message, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet on the address network if the global access state is not the modified state; wherein in response to the second type of packet, the system memory is configured to send a data packet corresponding to the coherency unit on the data network, regardless of whether the system memory has an ownership responsibility for the coherency unit.

However, Chandrasekaran teaches a multi-node network ***(figure 1)*** that employs several techniques to reduce latency. One of the methods is called an "optimistic read" ***(col. 2, lines 54 – 57)*** where the system sends the read data regardless of whether or not the data is valid (i.e. modified) ***(col. 2, lines 60 – 62)***. If a request made, its validity is determined. A message is sent

granting or denying access to the resource based on its validity. One of the methods of determining validity is "write-time" validity checking ***(col. 6, lines 25 – 36)***. When another node writes out data, it sends out a report stating the latest write time for that data. The read data is invalid once its timestamp comes before the latest write time. The node, now having an invalid read data, will now have to request the updated data from an additional node. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ optimistic reading of data using "write-time" validity checking so that reads could be employed when another node has exclusive access but hasn't yet written the data.

Also in regard to claims 1, 13, & 24 Liencres does not teach wherein the node has a data network that is separate from the address network. However, it is well known in the art to have separate data and address networks, as cited in Roy ***(col. 3, lines 61 – 67 through col. 4, lines 1 – 5)***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Liencres's invention by separating the network into separate address and data networks in order to improve performance using interleaving.

For claims 2, 14, & 25, Liencres teaches the coherency message requests a read access right to the coherency unit ***(see column 7, "Read Transactions")***, wherein the first type of address packet is a proxy read-to-share-modified packet ***(see figure 1d)*** and wherein the second type of address packet is a proxy memory read packet ***(see figure 1c)***.

For claim 3, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to send a data packet corresponding to the coherency unit to the interface via the data network in response to receipt of the proxy read-to-share-modified packet ***(see column 7, "Read Transactions")***.

For claim 15, Liencres teaches if the active device is the owner of the coherency unit, the active device is configured to send data corresponding to the coherency unit to the interface in response to receipt of the proxy read-to-share-modified packet ***(see column 7, "Read Transactions")***.

For claim 26, Liencres teaches an active device included in the node sending data corresponding to the coherency unit to the interface in response to receipt of the proxy read-to-share-modified packet if the active device has the ownership responsibility for the coherency unit ***(see column 7, "Read Transactions")***.

For claim 4, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to lose its ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet ***(see column 9, lines 22 – 31)***.

For claim 16, Liencres teaches if the active device is the owner of the coherency unit, the active device is configured to lose its ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet ***(see column 9, lines 22 – 31)***.

For claim 27, Liencres teaches the active device losing the ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet if the active device has the ownership responsibility for the coherency unit ***(see column 9, lines 22 – 31)***.

For claim 5, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to transition an access right to the coherency unit upon sending the data packet on the data network ***(see column 7, "Read Transactions")***.

For claims 6 & 22, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to a directory in point-to-point mode ***(see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode)***.

For claim 28, Liencres teaches the address network conveying the first and second types of address packet from the interface to a directory in point-to-point mode ***(see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode)***.

For claim 7, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to a plurality of devices included in the node in broadcast mode, wherein the plurality of devices include the system memory and the active device ***(see column 4, lines 45 – 49)***.

For claim 23, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to the plurality of devices in broadcast mode ***(see column 4, lines 45 – 49)***.

For claim 29, Liencres teaches the address network conveying the first and second types of address packet in broadcast mode ***(see column 4, lines 45 – 49)***.

For claims 8 & 21, Liencres teaches the data packet sent by the system memory includes an indication of the global access state of the coherency unit in the node ***(see column 7, lines 48 – 52)***.

For claim 9, Liencres teaches the coherency message requests a shared access right to the coherency unit ***(see figure 1d)***.

For claim 10, Liencres teaches the additional node is configured to send the coherency message in response to an additional active device included within the additional node sending

an address packet on an additional address network included within the additional node, wherein the address packet requests write access to the coherency unit, wherein the coherency unit is in a shared global access state in the additional node, and wherein the node is a home node of the coherency unit ***(see column 8, lines 63 – 68)***.

For claim 30, Liencres teaches the additional node sending the coherency message in response to an additional active device included within the additional node sending an address packet on an additional address network included within the additional node, wherein the address packet requests write access to the coherency unit, wherein the coherency unit is in a shared global access state in the additional node, and wherein the node is a home node of the coherency unit ***(see column 8, lines 63 – 68)***.

For claims 11 & 31, Liencres teaches if the coherency unit is in the shared global access state in any of the plurality of nodes other than the home node, the coherency unit is in the shared global access state in the home node and no active device and no memory subsystem included in any of the plurality of nodes has the ownership responsibility for the coherency unit ***(see figure 1a; see column 2, lines 15 – 24)***.

For claim 12, Liencres teaches the interface is configured to send a copy of the coherency unit included in the data packet to the additional node ***(see column 7, "Read Transactions")***.

For claim 20, Liencres teaches the data packet sent by the system memory includes a copy of the coherency unit ***(see column 7, "Read Transactions")***.

For claim 32, Liencres teaches the interface sending a copy of the coherency unit included in the data packet to the additional node ***(see column 7, "Read Transactions")***.

For claim 17, Liencres teaches the interface includes a global access state cache indicating global access states of a plurality of recently accessed coherency units in the node ***(see element 31)***.

For claim 18, Liencres teaches the interface is configured to check the global access state cache for the global access state of the coherency unit in the node, wherein if the global access state of the coherency unit is not included in the global access state cache, the interface is configured to request an indication of the global access state of the coherency unit from the system memory ***(see column 9, lines 14 – 31)***.

For claim 19, Liencres teaches the interface is configured to request the global access state of the coherency unit in the node from the system memory by sending the second type of address packet to the memory ***(see column 9, lines 14 – 31)***.

(10) Response to Argument

Appellant argues:

> ***Liencres "clearly shows that the memory alluded to ... is a cache memory 37, and not a system memory."***

and

> ***The bus cache controller 31, processor 21, and cache memory 37, are not interconnected as stated in the claim language.***

Examiner response:

The Appellant's disclosure does not draw such a clear picture that the memory in question is strictly a system memory. In section V of the "Summary of Claimed Subject Matter" of the Appeal Brief filed 05/27/08, the Appellant cites element 144A in figure 20 (4th line of the 1st paragraph of page 6) as the system memory. It's important to note that this memory ***is inside of each node*** (elements 140A-140C). The Examiner has cited element 37 as the memory, which is also inside of each node. There is no further definition of a system memory disclosed in the specification, but clearly states that memory 144A can store coherency units as cache lines (page 19, lines 4 – 11). Directory 220A is within memory 144A (figure 2). Further, the cache is "interconnected" through element 32, from which the memory 37 and the processor 21 are part of so the bus 33 does fit within the claim language.

Appellant argues:

> ***Read data in Chandrasekaran is sent without regard to validity, not ownership responsibility.***

and

> ***There is no teaching in Chandrasekaran of the interface sending one kind of packet if the coherency unit in the node is in a modified state and a second type of packet if it is not in a modified state.***

Examiner response:

Appellant's argument regarding Chandrasekaran sending read data "without regard to validity, and not whether the memory has ownership responsibility" is irrelevant. First validity shows the owner of the node because the node with write access is the owner. Second, as

Appellant points out, read data is "sent without regard to validity" (Appeal Brief page 12, line 3 of 2nd last paragraph). So, if data is sent without regard to validity, and validity shows the owner of the node, then it follows that sending without regard to validity is the same as sending without regard to ownership responsibility. Additionally, the type of packet that is sent is based on whether access is granted or denied.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,
/Shawn Eland/
Examiner, Art Unit 2188

Conferees:
/Hyung S Sough/
Supervisory Patent Examiner, Art Unit 2188
07/06/08

/Kevin L Ellis/
Acting SPE of Art Unit 2187
7/7/08